In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A data processing apparatus comprising:

a register file comprising a plurality of registers, each of said plurality of registers having a corresponding register number;

a first functional unit group connected to said register file and including a plurality of first functional units each having an output and further including an output multiplexer having a plurality of inputs receiving respective outputs of said first functional units and an output, said first functional unit group responsive to an instruction to

receive data from one of said plurality of registers corresponding to an instruction-specified first operand register number at an operand input,

operate on said received data employing an instruction-specified one of said first functional units, ~~and~~

select said output of said instruction-specified one of said first functional units via said output multiplexer, and

output data from said output of said output multiplexer to one of said plurality of registers corresponding to an instruction-specified first destination register number from an output;

a second functional unit group connected to said register file and including a plurality of second functional units each having an output and further including an output multiplexer having a plurality of inputs receiving respective outputs of said second functional units and an output, said second functional unit group responsive to an instruction to

receive data from one of said plurality of registers corresponding to an instruction-specified second operand register number at an operand input,

operate on said received data employing an instruction-specified one of said second functional units, ~~and~~

select said output of said instruction-specified one of said second functional units via said output multiplexer, and

output data from said output of said output multiplexer to one of said plurality of registers corresponding to an instruction-specified second destination register number from an output;

a first comparator receiving an indication of said first operand register number of a current instruction and an indication of said second destination register number of an immediately preceding instruction, said first comparator indicating whether said first operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a first register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said first comparator, said first register file bypass multiplexer having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said first functional unit group, said first multiplexer selecting said data from said register corresponding to said first operand number of said current instruction if said first comparator fails to indicate a match and selecting said output of said second functional unit group if said first comparator indicates a match;

said first functional units of said first functional unit group and said second functional units of said second functional unit group selected whereby functions often executed simultaneously within the same instruction cycle have corresponding functional units placed in different functional unit groups and functions which are not often executed together within the same instruction cycle have corresponding functional units placed in the same functional unit group.

2. (Previously Amended) The data processing apparatus of claim 1, wherein said register file, said first functional unit group, said second functional unit group, said first comparator and said first register file bypass multiplexer operate according to an instruction pipeline comprising:

a first pipeline stage consisting of a register read operation from said register file to provide operands for a selected functional unit of said first and second functional unit groups and a first half of operation of said selected functional unit of said first and said second functional unit groups, and

a second pipeline stage consisting of a second half of operation of said selected functional unit of said first and said second functional unit groups and a register write operation to said register file of results of operation of said selected functional unit of said first and second functional unit groups,

wherein the sum of the time of said register read operation and said register write operation equals approximately the sum of the time of said first and second halves of operation of a slowest of said functional units of said first and second functional unit groups.

3. (Previously Amended) The data processing apparatus of claim 1, further comprising an output register having an input

connected to said output of said second functional unit group and an output connected to said register file for temporarily storing said output of said second functional unit group prior to storing in said register corresponding to said second destination register number,

wherein said first comparator further receives an indication of said second destination register number of a second preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said second destination register number of said second preceding instruction, and

wherein said multiplexer further has a third input connected to said output register output, said multiplexer selecting said output register output if said first comparator indicates a match.

4. (Canceled)

5. (Previously Amended) The data processing apparatus of claim 1, said first comparator further receiving an indication of said first destination register of said immediately preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said first multiplexer further having a third input connected to said output of said first functional unit group, and said first multiplexer selecting said ~~first~~ output of said first functional unit group if said first comparator indicates a match.

6. (Previously Amended) The data processing apparatus of claim 1, said first functional unit group further responsive to an instruction to receive data from one of said plurality of registers

corresponding to an instruction-specified third operand register number at an operand input,

said apparatus further comprising:

a second comparator receiving an indication of said third operand register number of a current instruction and an indication of said second destination register number of said immediately preceding instruction, said second comparator indicating whether said third operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a second register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said second comparator, said second register file bypass multiplexer having a first input receiving data from said register corresponding to said third operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said first functional unit group, said second multiplexer selecting said data from said register corresponding to said third operand number of said current instruction if said second comparator fails to indicate a match and selecting said output of said second functional unit group if said second comparator indicates a match.

7. (Previously Amended) The data processing apparatus of claim 6, said first comparator further receiving an indication of said first destination register of said immediately preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said first multiplexer further having a third input connected to said output of said first functional unit

group, said first multiplexer selecting said output of said first functional unit group if said first comparator indicates a match,

said second comparator further receiving an indication of said first destination register of said immediately preceding instruction, said second comparator further indicating whether said third operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said second multiplexer further having a third input connected to said output of said first functional unit group, and said second multiplexer selecting said output of said first functional unit group if said second comparator indicates a match.

8. (Currently Amended) The data processing apparatus of claim 1, further comprising:

a second comparator receiving an indication of said second operand register number of a current instruction and an indication of said second destination register number of an immediately preceding instruction, said second comparator indicating whether said second operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a second register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said second comparator, said second register file bypass multiplexer having a first input receiving data from said register corresponding to said second operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said second functional unit group, said second multiplexer selecting said data from said register corresponding to said second operand number of

said current instruction if said second comparator fails to indicate a match and selecting said output of said second functional unit group if said second comparator indicates a match.

9. (Previously Amended) The data processing apparatus of claim 8, said second comparator further receiving an indication of said first destination register number of an immediately preceding instruction, said second comparator indicating whether said second operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said second multiplexer further having a third input connected to said output of said first functional unit group, and said second multiplexer further selecting said output of said first functional unit group if said second comparator indicates a match.

10. (Canceled)

11. (Currently Amended) A data processing apparatus comprising:

a first register file comprising a plurality of registers, each of said plurality of registers having a corresponding register number;

a second register file comprising a plurality of registers, each of said plurality of registers having a corresponding register number;

a first functional unit group including an input connected to said first and second register files, an output connected to said first register file, ~~and~~ a plurality of first functional units each having an output, and an output multiplexer having a plurality of inputs receiving respective outputs of said first functional units and an output, said first functional unit group responsive to an instruction to

receive data from one of said plurality of registers in said first and second register files corresponding to an instruction-specified first operand register number at an operand input,

operate on said received data employing an instruction-specified one of said first functional units, ~~and~~

select said output of said instruction-specified one of said first functional units via said output multiplexer, and

output data from said output of said output multiplexer to one of said plurality of registers in said first register file corresponding to an instruction-specified first destination register number from an output;

a second functional unit group including an input connected to said first and second register files, an output connected to said second register file, ~~and~~ a plurality of second functional units each having an output, and an output multiplexer having a plurality of inputs receiving respective outputs of said second functional units and an output, said second functional unit group responsive to an instruction to

receive data from one of said plurality of registers in said first and second register files corresponding to an instruction-specified second operand register number at an operand input,

operate on said received data employing an instruction-specified one of said second functional units, ~~and~~

select said output of said instruction-specified one of said second functional units via said output multiplexer, and

output data from said output of said output multiplexer to one of said plurality of registers in said second register file corresponding to an instruction-specified second destination register number from an output; and

a first crosspath connecting said second register file to said first functional unit group comprising

a first crosspath comparator, wherein, if said first operand register is in said second register file, said comparator receives an indication of said first operand register number of a current instruction and an indication of said second destination register number of a preceding instruction, and said first crosspath comparator indicates whether said first operand register number of said current instruction matches said second destination register number of said preceding instruction, and

a first crosspath multiplexer connected to said second register file, said first functional unit group, said second functional unit group and said first crosspath comparator, said first crosspath multiplexer having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said first functional unit group, wherein, if said first operand register is in said second register file, said first crosspath multiplexer selects said data from said register corresponding to said first operand number of said current instruction if said first crosspath comparator fails to indicate a match and selects said output of said second functional unit group if said first crosspath comparator indicates a match;

said first functional units of said first functional unit group and said second functional units of said second functional unit group selected whereby functions often executed simultaneously within the same instruction cycle have corresponding functional units placed in different functional unit groups and functions

which are not often executed together within the same instruction cycle have corresponding functional units placed in the same functional unit group.

12 to 17. (Canceled)

18. (Previously Added) The data processing apparatus of claim 2, wherein:

each first functional unit of said first functional unit group and each second functional unit of said second functional unit group includes a pipeline latch in the middle for latching a logical state of said functional unit between said first pipeline stage and said second pipeline stage.

19. (Canceled)

20. (New) The data processing apparatus of claim 11, wherein said register file, said first functional unit group, said second functional unit group, said first comparator and said first register file bypass multiplexer operate according to an instruction pipeline comprising:

a first pipeline stage consisting of a register read operation from said register file to provide operands for a selected functional unit of said first and second functional unit groups and a first half of operation of ~~a~~ said selected functional unit of said first and said second functional unit groups, and

a second pipeline stage consisting of a second half of operation of said selected functional unit of said first and said second functional unit groups and a register write operation to said register file of results of operation of said selected functional unit of said first and second functional unit groups,

wherein the sum of the time of said register read operation and said register write operation equals approximately the sum of the time of said first and second halves of operation of a slowest of said functional units of said first and second functional unit groups.

21. (New) The data processing apparatus of claim 20, wherein:

each first functional unit of said first functional unit group and each second functional unit of said second functional unit group includes a pipeline latch in the middle for latching a logical state of said functional unit between said first pipeline stage and said second pipeline stage.

22. (New) The data processing apparatus of claim 11, further comprising an output register having an input connected to said output of said second functional unit group and an output connected to said register file for temporarily storing said output of said second functional unit group prior to storing in said register corresponding to said second destination register number,

wherein said first comparator further receives an indication of said second destination register number of a second preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said second destination register number of said second preceding instruction, and

wherein said multiplexer further has a third input connected to said output register output, said multiplexer selecting said output register output if said first comparator indicates a match.

23. (New) The data processing apparatus of claim 11, said first comparator further receiving an indication of said first destination register of said immediately preceding instruction,

said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said first multiplexer further having a third input connected to said output of said first functional unit group, and said first multiplexer selecting said ~~first~~ output of said first functional unit group if said first comparator indicates a match.

24. (New) The data processing apparatus of claim 11, said first functional unit group further responsive to an instruction to receive data from one of said plurality of registers corresponding to an instruction-specified third operand register number at an operand input,

said apparatus further comprising:

a second comparator receiving an indication of said third operand register number of a current instruction and an indication of said second destination register number of said immediately preceding instruction, said second comparator indicating whether said third operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a second register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said second comparator, said second register file bypass multiplexer having a first input receiving data from said register corresponding to said third operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said first functional unit group, said second multiplexer selecting said data from said register corresponding to said third operand number of said current instruction if said second comparator fails to

indicate a match and selecting said output of said second functional unit group if said second comparator indicates a match.

25. (New) The data processing apparatus of claim 24, said first comparator further receiving an indication of said first destination register of said immediately preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said first multiplexer further having a third input connected to said output of said first functional unit group, said first multiplexer selecting said output of said first functional unit group if said first comparator indicates a match,

said second comparator further receiving an indication of said first destination register of said immediately preceding instruction, said second comparator further indicating whether said third operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said second multiplexer further having a third input connected to said output of said first functional unit group, and said second multiplexer selecting said output of said first functional unit group if said second comparator indicates a match.

26. (New) The data processing apparatus of claim 11, further comprising:

a second comparator receiving an indication of said second operand register number of a current instruction and an indication of said second destination register number of an immediately preceding instruction, said second comparator indicating whether said second operand register number of said current instruction

matches said second destination register number of said immediately preceding instruction; and

a second register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said second comparator, said second register file bypass multiplexer having a first input receiving data from said register corresponding to said second operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said second functional unit group, said second multiplexer selecting said data from said register corresponding to said second operand number of said current instruction if said second comparator fails to indicate a match and selecting said output of said second functional unit group if said second comparator indicates a match.

27. (New) The data processing apparatus of claim 26, said second comparator further receiving an indication of said first destination register number of an immediately preceding instruction, said second comparator indicating whether said second operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said second multiplexer further having a third input connected to said output of said first functional unit group, and said second multiplexer further selecting said output of said first functional unit group if said second comparator indicates a match.

28. (New) A data processing apparatus comprising:

a register file comprising a plurality of registers, each of said plurality of registers having a corresponding register number;

a first functional unit group connected to said register file and including a plurality of first functional units, said first functional unit group responsive to an instruction to

receive data from one of said plurality of registers corresponding to an instruction-specified first operand register number at an operand input,

operate on said received data employing an instruction-specified one of said first functional units, and

output data to one of said plurality of registers corresponding to an instruction-specified first destination register number from an output;

a second functional unit group connected to said register file and including a plurality of second functional units, said second functional unit group responsive to an instruction to

receive data from one of said plurality of registers corresponding to an instruction-specified second operand register number at an operand input,

operate on said received data employing an instruction-specified one of said second functional units, and

output data to one of said plurality of registers corresponding to an instruction-specified second destination register number from an output;

a first comparator receiving an indication of said first operand register number of a current instruction and an indication of said second destination register number of an immediately preceding instruction, said first comparator indicating whether said first operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a first register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said first comparator, said first

register file bypass multiplexer having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said first functional unit group, said first multiplexer selecting said data from said register corresponding to said first operand number of said current instruction if said first comparator fails to indicate a match and selecting said output of said second functional unit group if said first comparator indicates a match;

said first functional units of said first functional unit group and said second functional units of said second functional unit group selected whereby functions often executed simultaneously within the same instruction cycle have corresponding functional units placed in different functional unit groups and functions which are not often executed together within the same instruction cycle have corresponding functional units placed in the same functional unit group; and

wherein said register file, said first functional unit group, said second functional unit group, said first comparator and said first register file bypass multiplexer operate according to an instruction pipeline comprising:

a first pipeline stage consisting of a register read operation from said register file to provide operands for a selected functional unit of said first and second functional unit groups and a first half of operation of said selected functional unit of said first and said second functional unit groups, and

a second pipeline stage consisting of a second half of operation of said selected functional unit of said first and said second functional unit groups and a register write operation to said register file of results of operation of said selected functional unit of said first and second functional unit groups,

wherein the sum of the time of said register read operation and said register write operation equals approximately the sum of the time of said first and second halves of operation of a slowest of said functional units of said first and second functional unit groups.

29. (New) The data processing apparatus of claim 28, further comprising an output register having an input connected to said output of said second functional unit group and an output connected to said register file for temporarily storing said output of said second functional unit group prior to storing in said register corresponding to said second destination register number,

wherein said first comparator further receives an indication of said second destination register number of a second preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said second destination register number of said second preceding instruction, and

wherein said multiplexer further has a third input connected to said output register output, said multiplexer selecting said output register output if said first comparator indicates a match.

30. (New) The data processing apparatus of claim 28, said first comparator further receiving an indication of said first destination register of said immediately preceding instruction, said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said first multiplexer further having a third input connected to said output of said first functional unit group, and said first multiplexer selecting said ~~first~~ output of said first functional unit group if said first comparator indicates a match.

31. (New) The data processing apparatus of claim 28, said first functional unit group further responsive to an instruction to receive data from one of said plurality of registers corresponding to an instruction-specified third operand register number at an operand input,

said apparatus further comprising:

a second comparator receiving an indication of said third operand register number of a current instruction and an indication of said second destination register number of said immediately preceding instruction, said second comparator indicating whether said third operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a second register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said second comparator, said second register file bypass multiplexer having a first input receiving data from said register corresponding to said third operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said first functional unit group, said second multiplexer selecting said data from said register corresponding to said third operand number of said current instruction if said second comparator fails to indicate a match and selecting said output of said second functional unit group if said second comparator indicates a match.

32. (New) The data processing apparatus of claim 31, said first comparator further receiving an indication of said first destination register of said immediately preceding instruction, said first comparator further indicating whether said first operand

register number of said current instruction matches said first destination register number of said immediately preceding instruction, said first multiplexer further having a third input connected to said output of said first functional unit group, said first multiplexer selecting said output of said first functional unit group if said first comparator indicates a match,

said second comparator further receiving an indication of said first destination register of said immediately preceding instruction, said second comparator further indicating whether said third operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said second multiplexer further having a third input connected to said output of said first functional unit group, and said second multiplexer selecting said output of said first functional unit group if said second comparator indicates a match.

33. (New) The data processing apparatus of claim 28, further comprising:

a second comparator receiving an indication of said second operand register number of a current instruction and an indication of said second destination register number of an immediately preceding instruction, said second comparator indicating whether said second operand register number of said current instruction matches said second destination register number of said immediately preceding instruction; and

a second register file bypass multiplexer connected to said register file, said first functional unit group, said second functional unit group and said second comparator, said second register file bypass multiplexer having a first input receiving data from said register corresponding to said second operand register number of said current instruction, a second input

connected to said output of said second functional unit group and an output supplying an operand to said operand input of said second functional unit group, said second multiplexer selecting said data from said register corresponding to said second operand number of said current instruction if said second comparator fails to indicate a match and selecting said output of said second functional unit group if said second comparator indicates a match.

34. (New) The data processing apparatus of claim 33, said second comparator further receiving an indication of said first destination register number of an immediately preceding instruction, said second comparator indicating whether said second operand register number of said current instruction matches said first destination register number of said immediately preceding instruction, said second multiplexer further having a third input connected to said output of said first functional unit group, and said second multiplexer further selecting said output of said first functional unit group if said second comparator indicates a match.

35. (New) The data processing apparatus of claim 28, wherein:

each first functional unit of said first functional unit group and each second functional unit of said second functional unit group includes a pipeline latch in the middle for latching a logical state of said functional unit between said first pipeline stage and said second pipeline stage.